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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shekhar Y. Borkar et al. Art Unit : 2816
Serial No.: 09/802,584 Examiner : Cassandra Cox
Filed : March 8, 2001
Title : A SYNCHRONOUS CLOCK GENERATOR FOR INTEGRATED CIRCUITS

BOX AF

Commissioner for Patents
Washington, D.C. 20231

Do Not Enter
8/19/02

RESPONSE

In response to the action mailed April 22, 2002, please amend the application as follows:

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10/9/02

In the claims:

Please amend claims 1, 9, and 14 as follows:

-- 1. (Amended) A device, comprising:

a delay lock loop circuit responsive to an input signal to delay the input signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to the input signal, the delay circuit being responsive to the analog control signal from the delay lock loop

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

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Tobi Terry

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Washington, D.C. 20231TRANSMITTAL LETTER

Correspondence relating to this application is enclosed.

The required fees are computed below. Please apply any charges not covered, or any credits, to Deposit Account No. 06-1050.

Total Claims	20	-	20	=	0	\$0
Independent	3	-	3	=	0	\$0
TOTAL FEE DUE						\$0

No fee is due at this time.

Respectfully submitted,

Joseph L. Stevenson
Reg. No. 43,163

Date: July 22, 2002

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